Notice of Allowability	Application No.	Applicant(s)	
	10/059,554	BRADLEY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/28/2007*.

2. ☒ The allowed claim(s) is/are *2, 8-9, 12-13, 15-16, 18-19, and 22-25, as renumbered as 1-13*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *attached herein* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Anthony V.S. England, Reg. No. 35,129 on 06/04/2007.

The application has been amended claims 8 and 13 for typo correction as follows:

8. (Currently Amended) The adder circuit of claim 22~~-3~~, wherein the at least one tier of group circuits includes a first tier of group circuits configured to receive the output of the PGK circuits and to generate an intermediate set of group propagate, generate, and kill values, and a second tier of at least one group circuit configured to receive the intermediate set of group propagate, generate, and kill values and to produce a final group propagate, generate, and kill values.

13. (Currently Amended) A microprocessor including <u>an</u> ~~and~~ adder circuit for determining the sum of two operands, the adder comprising:

a set of PGK circuits configured to generate propagate, generate, and kill bits corresponding to at least a portion of the first and second operands;

at least one tier of group circuits configured to receive the propagate, generate, and kill bits from a plurality of the PGK circuits and to produce, in response thereto, a set of group propagate, generate, and kill values;

a carry generation circuit configured to receive a carry-in bit and the outputs of at least one of the group circuits and further configured to generate a carry-out bit representing the carry-out of the corresponding group; and

a select circuit configured to select between a first sum and a second sum responsive to the carry-out bit

wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one complementary metal oxide semiconductor transmission gate;

wherein the complementary metal oxide semiconductor transmission circuit comprises a PMOS transistor and an NMOS transistor, wherein a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and

wherein a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor; and

wherein a gate terminal of the PMOS transistor is driven by a first signal and a gate terminal of the NMOS transistor is driven by the logical complement of the first signal.

2. Claims 2, 8-9, 12-13, 15-16, 18-19, and 22-25 are allowed.

3. Claims 1, 3-7, 10-11, 14, 17, and 20-21 are cancelled.

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of an adder circuit for summing two operands comprising: a set of PKG circuits; at least one tier of group circuits configured to receive the PKG from the PKG circuits; a carry generation circuit configured to generate a carry output bit; and a select circuit configured to output sum responsive to the carry-output bit; wherein at least one of the PGK circuits, group circuits, and carry circuits includes at least one complementary metal oxide semiconductor transmission gate; wherein the complementary metal oxide semiconductor transmission circuit comprises a PMOS transistor and an NMOS transistor, wherein a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and wherein a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor; and wherein a gate terminal of the PMOS transistor is driven by a first signal and a gate terminal of the NMOS transistor is driven by the logical complement of the first signal along with other limitations cited in independent claims 13 and 22.

The closest found prior art is Hayakawa (U.S. Publication No. 2001/0037349). Hayakawa also discloses an adder circuit for summing two operands comprising PKG circuits, but either fails to explicitly, expressively, or inherently disclose at least one of the PGK circuits, group circuits, and carry circuits includes at least one complementary metal oxide semiconductor transmission gate; wherein the complementary metal oxide semiconductor transmission circuit comprises a PMOS transistor and an NMOS

transistor, wherein a first source/drain terminal of the PMOS transistor is connected to a first source/drain terminal of the NMOS transistor and wherein a second source/drain terminal of the PMOS transistor is connected to a second source/drain terminal of the NMOS transistor; and wherein a gate terminal of the PMOS transistor is driven by a first signal and a gate terminal of the NMOS transistor is driven by the logical complement of the first signal as seen in above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chat C. Do
Examiner
Art Unit 2193

June 6, 2007

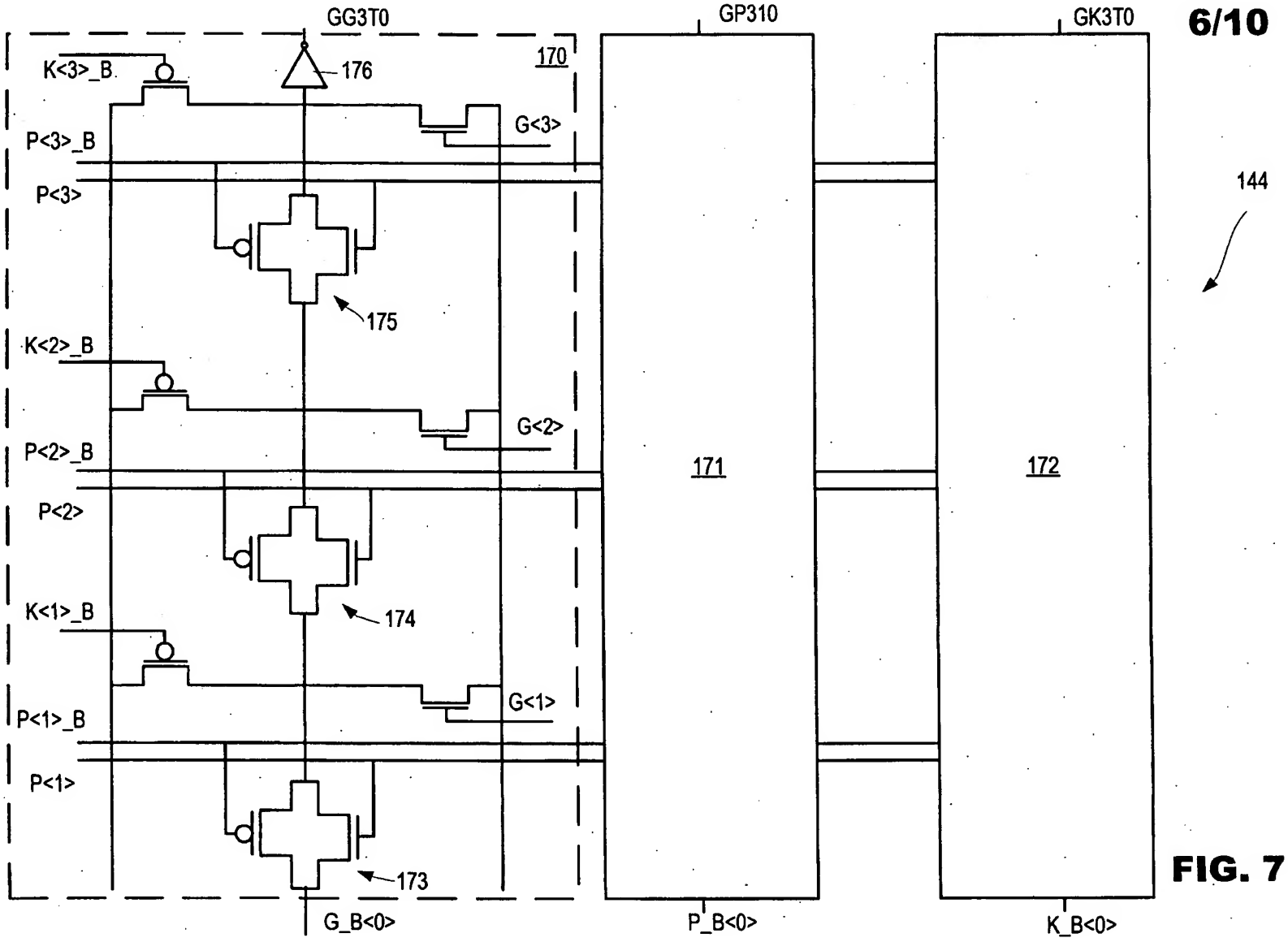

FIG. 7

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